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09/733,243	12/07/2000	Robert Louis Hodges	98-P-104C1 (850063.542C1)	7298

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EXAMINER
TRINH, MICHAEL MANH

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/733,243	Applicant(s) HODGES, ROBERT LOUIS	
	Examiner Michael Trinh	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-24 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-24 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

*** This office action is in response to Applicant's amendment filed on January 03, 2003. Claims 14-24 and 26 are currently pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

1. Claims 14-24 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re base claims 14 and 21: Using different terms to recite the same layer render meaning and scope of the claims, if not new matter, being unclear, confusing and indefinite. For example of the inconsistency: a) Claim 14 recites "forming an opening extending through said first layer..." while claim 21 differently recites "forming an opening...and not through said first layer..." and while specification Fig 1 recites "opening through the third layer..."; and b) Claim 14 recites "forming a second layer in the gap..." while claim 21 differently recites "forming a fourth layer in the gap...", etc.

(Dependent claims are rejected as depending on rejected base claim.

Claim Rejections - 35 USC § 103

2. Claims 14,17,20,21,22,23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao et al (5,688,700) taken with Yu et al (6,190,980) and Hook et al (6,271,565).

Re claim 14, Kao teaches a method (at figs 1-16; cols 4-5) for forming feature having a critical selected dimension comprising at least the steps of: forming a first layer 22 (Fig 7) having a first thickness; forming an opening 24 having vertical sidewalls separated by a width greater than the critical dimension 25 extending through the first layer 22; forming a blanket dielectric layer 28 (Fig 8; col 4, lines 50-60) having a second thickness in the opening, on the first layer and on the sidewalls, the second thickness being half or less of the first thickness; selectively and anisotropically etching the blanket dielectric layer to form dielectric spacers 30

(Fig 9; col 4, lines 61+) on the sidewalls and to remove the blanket dielectric layer from a bottom of the opening without etching the first layer, the dielectric spacers 30 separated by a gap having a width equal to the critical dimension; forming a second layer 36 (Fig 13) in the gap and on the first layer; removing those portions of the second layer formed on the first layer using a chemical-mechanical polish without removing portions of the second layer in the gaps (Fig 14; col 5, lines 26-41); and removing the first layer 22 but not the dielectric spacers 30 (Figs 15-16). Re claim 21, Kao teaches forming a first layer 20 (Fig 7) having a first thickness on a semiconductor substrate 12; forming a second layer 22 over the first layer 20, the second layer having a second thickness thicker than the first layer and being etchable by a different etch chemistry than the first layer 20; forming a recess opening 24 having vertical sidewalls separated by a width greater than the critical selected dimension 25 extending through the second layer 22 and not through the first layer 20 (Fig 7); forming a blanket dielectric layer 28 (Fig 8; col 4, lines 50-60) having a third thickness in the opening, on the second layer 22 and on the sidewalls, and on top of the first layer in the recess opening, the third thickness being half or less of the second thickness; selectively and anisotropically etching the blanket dielectric layer to form dielectric spacers 30 (Fig 9; col 4, lines 61+) on the sidewalls and to remove the blanket dielectric layer from a bottom of the recess opening; etching the first layer 20 to expose the substrate (Figs 10-11) and form a gap having a width equal to the critical selected dimension between the dielectric spacers 30; forming a fourth layer 36 (Fig 13) in the gap and on the substrate (Fig 14; col 5, lines 26-41); and removing any remaining portions of the second layer 22 without removing the dielectric spacers 30 (Figs 15-16). Re claim 17, wherein the blanket dielectric layer 28 is silicon nitride (col 4, lines 55-60). Re claims 22-23, wherein forming the first layer having a first thickness comprises forming two chemically distinct sub-layers and selectively etchable on the surface of the substrate, wherein forming the first layer comprises forming a thermal oxide 14 on the substrate of silicon; and forming a silicon nitride layer 20 having a thickness of less than five hundred Angstroms on the thermal oxide 14.

Kao et al lacks implanting ions under the dielectric spacer at an angle (claim 14) or at multiple angles (claims 21 and 26).

However, Yu et al teach (at col 2, line 57 through col 3, line 5; col 4, lines 10-18; Figs 3-4) forming halo regions by successively creating tilted implants, wherein ions are implanted into

the substrate at a location beneath the opening, wherein implantation is performed at multiple angles so as to provide implanted ions under the dielectric spacers on each side of the opening, and wherein implanting angles are oppositely shown in Figure 3 with respect to the perpendicular line. Hook et al teach implanting ions into the substrate at a location beneath the opening (col 1, lines 25-32; Figs 1-4; col 5, lines 15-30), wherein the implanting is performed at a series of symmetrical implants at multiple angles to provide implanted ions under the dielectric spacers on each side of the opening in order to form halo regions.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the method of Kao et al by implanting ions at a series of symmetrical implants at multiple angles to provide implanted ions under the dielectric spacers on each side of the opening, as taught by Yu and Hook. This is because of the desirability to form the halo regions for preventing punch through effects as well known in the semiconductor art.

3. Claims 15,16,19,24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao et al (5,688,700) taken with Yu et al (6,190,980) and Hook et al (6,271,565), as applied above to claims 14,17,20,21,22,23 and 26, and further of Niwa (5,597,752) or Chau et al (5,434,093).

Kao teaches a method (at figs 1-16; cols 4-5) for forming feature having a critical selected dimension as applied above to claims 14,17,20,21,22,23. Re further claims 15,16,14, Kao also teaches to form a series of chemically distinct sub-layers and selectively etchable on the surface of the substrate, wherein forming the first layer comprises forming a thermal oxide 14 on the substrate of silicon; forming a silicon nitride layer 20 having a thickness of less than five hundred Angstroms on the thermal oxide 14; and forming a silicon oxide layer 22 having a thickness on the silicon nitride layer. Re further claim 19, Kao also teaches to pre-cleaning by stripping the pad oxide 14; forming gate oxide layer 34 on the substrate within the gap (col 5, lines 19-25); forming a channel within the gap (figs 10-16); forming the second layer 36 of conductive material (fig 13), and chemical-mechanical polishing to remove the second layer from the first layer 22 (col 5, lines 26-54).

Re claims 15,16,24, Kao teaches to form the silicon oxide top layer, but lacks to mention a thickness of five thousand Angstroms or less.

Niwa teaches (at col 5, lines 51-15) to form the silicon oxide top layer 4 having a thickness of about 5000 Angstroms. Chau et al teach (at col 7, lines 25-67) to select the insulating layer 201 of silicon nitride or oxide (col 7, lines 64-68) having a thickness within the range of approximately 0.05 to 1 microns (500-10000 Angstroms), wherein 2000-4000 Angstroms is mentioned at col 7, lines 23-35.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the silicon oxide top layer of Kao by selecting the portion of the prior art's thickness range, as taught by Niwa and Chau, which is within the range of applicant's claims because it has been held to be obvious to select a value in a known range by optimization for the best results, see In re Aller, etal., 105 USPQ 233.

Re claim 19, Kao forms the gate oxide top layer, but lacks to mention thermally growing.

However, Niwa teaches (at col 6, lines 15-28; Figs 4E-4F) to pre-cleaning by etching the oxide layer 2 and then thermally growing a new gate silicon oxide layer 7. Chau et al teach (at Figs 2e-2f; col 10, lines 16-41) to cleaning the substrate and thermally growing a gate oxide 212 in the gap.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate oxide of Kao by pre-cleaning and thermally growing a new gate oxide in the gap as taught by Niwa and Chau. This is because of the desirability to selectively forming a high quality gate oxide in the gap.

4. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kao et al (5,688,700) taken with Yu et al (6,190,980) and Hook et al (6,271,565), as applied above to claims 14,17,20,21,22,23 and 26, and further of Wolf et al (Page 192, second paragraph).

The relied references including Kao teaches a method (at figs 1-16; cols 4-5) for forming feature having a critical selected dimension as applied above to claims 14,17,20,21,22,23.

Re claim 18, Kao teaches to form the blanket dielectric layer of the silicon nitride, but lacks to mention using LPCVD.

However, Wolf teaches (at page 192,) to use LPCVD for depositing the silicon nitride.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the silicon nitride layer of Kao by using LPCVD as taught by Wolf et al for reasons of film uniformity and lower processing cost.

5. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kao et al (5,688,700) taken with Yu et al (6,190,980) and Hook et al (6,271,565), as applied above to claims 14,17,20,21,22,23 and 26, and further of Goth et al (4,58,528).

The relied references including Kao teaches a method (at figs 1-16; cols 4-5) for forming feature having a critical selected dimension as applied above to claims 14,17,20,21,22,23.

Re claim 25, Kao lacks to remove remaining second layer prior to forming fourth layer.

However, Goth teaches (at figs 5A-5B; cols 7-8) to remove remaining second layer 53/54 (Figs 5C-5D) prior to forming a fourth layer 57 in the gap (Fig 5E)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Kao by remove any remaining second layer prior to form a fourth layer in the gap as taught by Goth et al for reasons of forming a plurality electrode layer at the same time and thus reducing processing time.

Response to Arguments

6. Applicant's remarks filed January 03, 2003 have been fully considered but they are not persuasive, and to are also moot in view of the new ground(s) of rejection.

** Regarding 35 USC 112 rejection:

Applicant mainly alleged that "...these remarks are part of the file wrapper history...will clearly understand the invention as claimed...".

In response, per Applicant's remark, it is agreed that "file wrapper history" is used to understand the claimed invention. However, the remarks are not printed on the Patent, it is still unclear and confusing to read and understand the claims having these inconsistent claimed terms. Applicant apparently requires that every patent readers must order the application and read "file wrapper history" in order to simply understand every Applicant's claims.

As can be seen, for the same thing, Claim 14 recites "forming an opening extending through said first layer..." while claim 21 differently recites "forming an opening...and not

through said first layer..." and while specification Fig 1 recites "opening through the third layer...". Therefore, it is maintained that using different terms to recite the same thing renders meaning and scope of the claims being unclear and confusing even in light of the specification. Using of the claimed languages are inconsistent.

** Regarding art rejections:

As described above in the rejections, Yu or Hook prima facie teaches forming halo regions by successively creating tilted implants, wherein ions are implanted into the substrate at a location beneath the opening, and wherein implantation is performed at multiple angles so as to provide implanted ions under the dielectric spacers on each side of the opening.

****

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs

Michael Trinh
Primary Examiner